WHAT IS CLAIMED IS:

1. A semiconductor memory device inputting/outputting data in a burst operation, comprising:

a memory cell array having a plurality of memory cells;

a row decoder decoding a row address;

a first column decoder decoding a column address;

a second column decoder decoding a column address for parity; and

a control unit controlling said first column decoder and said second column decoder, such that parity data is input/output to/from said memory cell array at a timing different from that of input/output of data corresponding to/from said parity data to said memory cell array.

2. The semiconductor memory device according to claim 1, wherein said control unit controls said first column decoder so as to control writing of data in a prescribed number of burst operations, and thereafter, controls said second column decoder so as to control writing of parity data corresponding to said data.

3. The semiconductor memory device according to claim 1, wherein said control unit controls said second column decoder so as to control reading of parity data, and thereafter, controls said first column decoder so as to control reading of data corresponding to said parity data in a prescribed number of burst operations.

4. The semiconductor memory device according to claim 1, wherein said second column decoder decodes a portion of an address decoded by said first column decoder.

5. A controller controlling a semiconductor memory device inputting/outputting data in a burst operation, comprising:

a buffer holding parity data input/output to/from said semiconductor memory device, and shifting the parity data by a prescribed bit unit;

an operation unit calculating parity data for data written in a prescribed number of burst operations with respect to said semiconductor memory device, to sequentially store the parity data in said buffer by a prescribed bit unit, and sequentially reading parity data from said buffer by the prescribed bit unit in accordance with data read in the prescribed number of burst operations with respect to said semiconductor memory device, to correct an error; and

a switching unit controlling input/output of the parity data to/from said buffer.

6. The controller according to claim 5, wherein

said switching unit outputs parity data corresponding to the data stored in said buffer, after burst writing of the prescribed number of times with respect to said semiconductor memory device is completed.

7. The controller according to claim 5, wherein

said switching unit outputs parity data corresponding to the data to said buffer, before burst reading of the prescribed number of times with respect to said semiconductor memory device is performed.